ECE 342 Experiment 5
Single Transistor Amplifiers

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Abstract

In this experiment, two discrete transistor amplifiers are designed, simulated, and built. The first amplifier is a common emitter amplifier and the second is a common gate amplifier. Each circuit is designed to have a specified frequency response. Along with designing the amplifiers, the impact of various load impedance's on the input and output are investigated through simulations and measurements. The common emitter is designed to pass frequencies above 2kHz, and the common gate is designed to pass frequencies above 1kHz. The common emitter is designed to have a gain of 40dB. No gain was specified for the common gate amplifier. The common gate amplifier had a gain of 36dB.

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1 Introduction

In this lab experiment two styles of discrete transistor amplifiers are explored − the Bipolar Junction Transistor (BJT) based common emitter (CE) amplifier and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) based common gate (CG) amplifier. The two amplifiers will have different methods of biasing. For the CE based amplifiers, the biasing circuit is built using a 1mA current mirror, and the CG will use a traditional resistor based biasing network.

An ideal amplifier is one that has infinite input resistance, zero output resistance and a constant frequency response. The discrete transistor amplifiers explored in this experiment are the foundational amplifying circuits, which, when used in tandem can provide near−ideal amplification (i.e. op−amps, power amplifiers etc.), even though these circuits produce non ideal amplifiers. The method of using multiple amplifiers in tandem to produce better amplifier is not explored in this lab, it is mentioned to provide context to what is being performed.

The operating conditions and specifications for the circuits are provided in the lab manual as follows[1]. The CE amplifier must have an unloaded voltage gain , A_{vo}, greater than 40dB, or 100V/V. The bias network must be designed such that V_B is −1.5V ±0.3V, and the current flowing through R_{B1} is between 100μA and 200μA. The node voltage V_C must be 1.0V ±0.5V. The collector current I_C must be 1mA±0.2mA. Lastly, the emitter capacitor must be chosen such that the lower cut−off frequency of the amplifier, f_{LO}, is less than 2kHz. The CG amplifier does not have a gain specification, instead only the specification for the lower cut−off frequency f_{LO} must be below 1kHz.

This document is split into three sections. Section 2 features the circuit design and analysis. This section contains calculations for the common emitter and common gate amplifiers. Section 3 includes the simulations. Here, the designed circuits are simulated to validate they are acting as an amplifier. Section 4 features the experimental implementation, where each circuit is built and tested. In the experimental section, each circuit is built and measurements are taken to validate the expected values from the designs and simulations section.

2 Circuit Design and Analysis

Both circuits designed are amplifier circuits. They take an AC input signal and amplify it at the output. There are three primary types of amplifiers, voltage, current, and power amplifiers. An amplifier can be characterized by its input resistance, output resistances and unloaded gain (A_{VO}). The unloaded gain describes the amount of amplification applied to the signal in terms of volts per volt (V/V) − often converted to decibels. Both circuits designed in this experiment are voltage amplifiers. The first being a common emitter amplifier and the second being a common gate amplifier. The common emitter is a BJT circuit with the input applied at the base, and the output taken from the source. For this circuit, small signal parameters, component values and amplifier characteristics will be calculated. The unloaded voltage gain must be above 40dB. This specification sets a bound on the value of the collector resistor R_C. The other bound is set by the collector voltage specification of 1.0 ±0.5V. The base resistor network (R_{B1} and R_{B2}) must be designed such that the base voltage, V_B, is 1.0V ±and the current through R_{B1} is between

100μA and 200μA. The required collector current of 1mA$\pm$0.2mA is supplied by the current mirror built in Experiment 4. Because the amplifier has a band pass characteristic, C_E must be chosen such that the lower cutoff frequency is below 2kHz. Also, the amplifier input and output resistances will be determined. The common gate amplifier has less specifications because it is simply an extension of the MOSFET biased circuit from Experiment 4. Here, the supply voltages must be $\pm$12V and the drain to source current I_{DS} must be 1mA$\pm$0.2mA. The source capacitor C_S must be chosen such that the lower cutoff frequency is below 1kHz. Once the component values for each amplifier are determined, their small signal parameters are calculated.

2.1 Common Emitter Amplifier

Figure 1 shows the schematic for the common emitter amplifier.

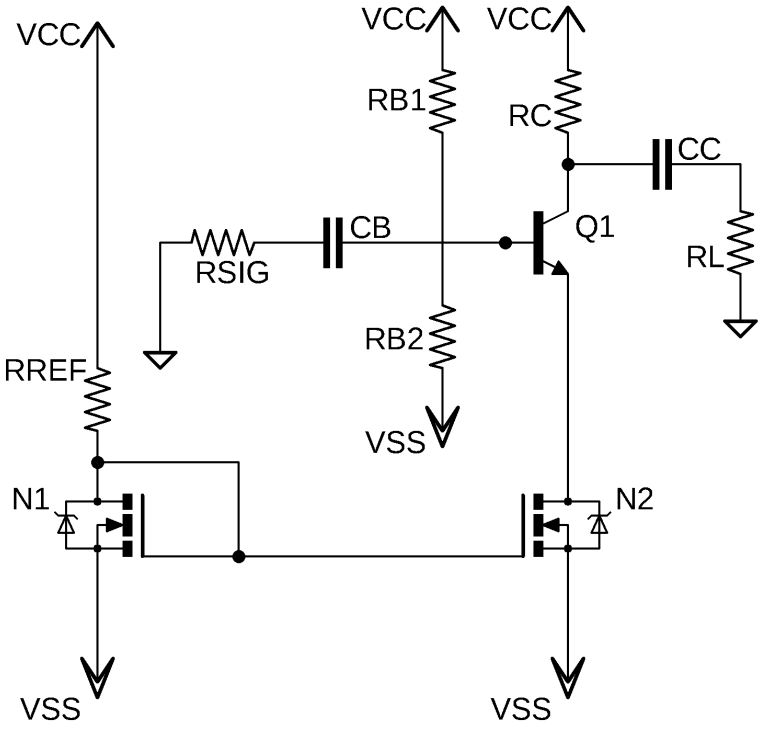

Fig. 1. Common Emitter amplifier circuit schematic

The BJT used in this circuit is the ON Semiconductor 2N3904.

2.1.1 Collector Resistor

The collector resistor R_C will be calculated to set the unloaded voltage gain above 40dB. The collector resistor has two equations to determine an allowable range of values. To determine the lower bound of the resistor value Equation 1, the unloaded voltage gain, is used.

$$A_{VO} = \frac{I_C}{V_T} * R_C \tag{1}$$

Here, A_{VO} must be above 100V/V, I_C is 1mA, and V_T is the thermal voltage of 26mV. Using these values, the lower bound of R_C is 2600Ω. The upper bound is set by the collector voltage specification of 1.0V$\pm$0.5V. The voltage across the resistor R_C can be written as seen in Equation 2.

$$V_{RC} = V_{DD} - V_C = I_C * R_C \tag{2}$$

Here, V_DD is 5V, V_C is 1V, and I_C is 1mA. Solving for R_C results in an upper bound of 4000Ω on the value of R_C. The mid point of the range is chosen for the value of R_C resulting in a value of 3.3kΩ.

2.1.2 Base Network Resistors

The base network resistor R_{B1} can be determined using equation 3.

$$R_{B1} = \frac{V_{DD} - V_B}{I_{R_{B1}}} \tag{3}$$

Here, the supply voltage V_{DD} is 5V, V_B is specified to be -1.5V, and $I_{R_{B1}}$ is specified to be between 100muA and 200muA, resulting in 150muA. These values result in an R_{B1} value of 43kΩ. The second base network resistor can be determined by the following equation.

$$V_B = \frac{V_{DD} - (V_{DD} - (-V_{EE})}{R_{B2} + R_{B1}} * R_{B1} \tag{4}$$

Here, the supply voltages V_{DD} and $-V_{SS}$ are $\pm$5V, V_B is -1.5V, and R_{B1} is 43kΩ. R_{B2} can then be solved for, resulting in a value of 23.7kΩ.

2.1.3 Collector Capacitor

The collector capacitor C_E can be determined from the following equation.

$$f_{LO} \approx \frac{1}{2 * \pi * C_E * r_{e_{Q1}}} \tag{5}$$

Here, f_{LO} must be below 2kHz, $r_{e_{Q1}}$ is a small signal parameter of the amplifier and is determined as follows.

$$r_{e_{Q1}} = \frac{V_T}{I_C} \tag{6}$$

Here, V_T is 26mV and I_C is 1mA. This results in $r_{e_{Q1}}$ equal to 26Ω. Using this value in to equation 5 results in C_E equal to 4.7uF.

2.1.4 Small Signal Parameters

With all component values determined, the small signal parameters of the amplifier can be determined. The small signal model resistors are denoted by a lowercase r. r_e is found above to be 26Ω. r_π is calculated as follows.

$$r_\pi = \frac{\beta * V_T}{I_C} \tag{7}$$

Here, β is 200, V_T is 26mV, and I_C is 1mA. These values result in r_π = 5200Ω. r_o is calculated with the following equation.

$$r_o = \frac{V_A}{I_C} \tag{8}$$

With V_A equal to 75V, and I_C equal to 1mA, r_o is 75kΩ. The small signal transconductance determines the unloaded voltage gain and is determined as follows.

$$g_m = \frac{I_C}{V_T} \tag{9}$$

With I_C equal to 1mA and V_T equal to 26mV, g_m is equal to $38.5\frac{mA}{V}$.

2.1.5 Amplifier Characteristics

With all components and small signal parameters calculated, the amplifier characteristics can be determined. The input resistance R_{IN} is determined by the parallel combination of the resistors r_pi, R_{B1}, and R_{B2}. With r_π equal to 26Ω, R_{B1} equal to 43kΩ, and R_{B2} equal to 23.7kΩ, R_{IN} equals 3879Ω. The output resistance R_{OUT} is the parallel combination of the resistor r_o and R_C. With r_o equal to 75kΩ, and R_C equal to 3.3kΩ, R_{OUT} is 3.161kΩ. Lastly, the unloaded voltage gain can again be calculated to ensure it meets specifications.

$$A_{VO} = -g_m * R_C \tag{10}$$

With g_m equal to 38.5mA and R_C equal to 3.3kΩ, A_{VO} equals $-127.05\frac{V}{V}$ or 42.07dB, meeting the minimum specified gain of 40dB.

2.2 Common Gate Amplifier

The common gate amplifier required less calculations as it was simply a modification of the biased MOS−FET circuit built in Experiment 4. Figure 2 shows the schematic for the common emitter amplifier.

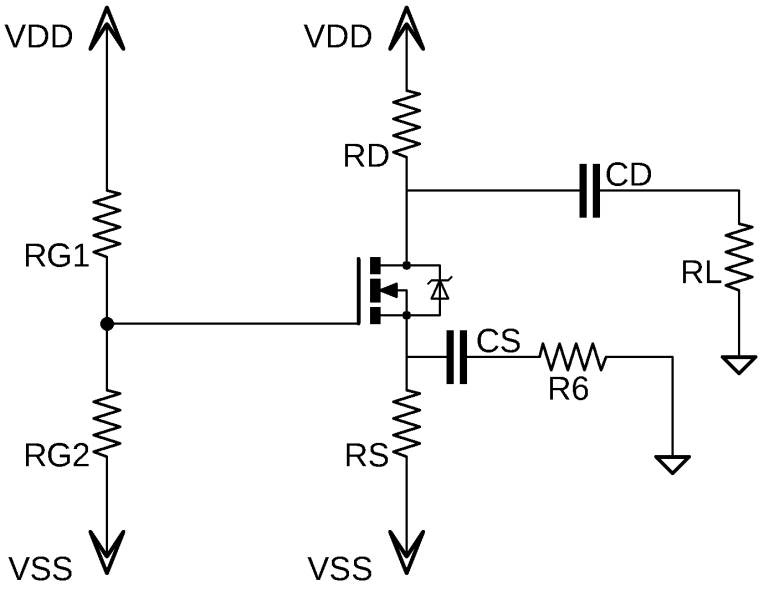

Fig. 2. Common Gate amplifier circuit schematic

The MOSFET used in this circuit is the ON Semiconductor 2N7000.

2.2.1 Small Signal Parameters

The small signal transconductance can be calculated using the following equation.

$$g_m = \sqrt{2 * k_n * I_{DS}} \tag{11}$$

k_n for the 2N7000 is $100\frac{mA}{V^2}$, and I_{DS} is 1mA, resulting in g_m equal to $14.14\frac{mA}{V}$. r_s is equal to the reciprocal of the small signal transconductance, and is therefore 70.7Ω.

2.2.2 Source Capacitor

The source capacitor C_S can be determined using the following equation.

$$C_S > \frac{1}{2 * \pi * f_{LO} * (r_s + R_{SIG}} \tag{12}$$

R_{SIG} is set to be 0Ω, r_s is equal to 70.7Ω, and f_{LO} must be higher than 1kHz. With those values, C_S is 4.7μA. This results in a f_{LO} of 479Hz, within the specified range of below 1kHz.

2.2.3 Amplifier Characteristics

The input resistance of the amplifier is the parallel combination of r_s and R_S. This results in R_{IN} equal to 68.02Ω. The output resistance is equal to resistor R_D, resulting in R_{OUT} equal to 10kΩ. The unloaded voltage gain can be calculated using the following equation.

$$A_{VO} = g_m * R_D \tag{13}$$

With g_m equal to $14.14\frac{mA}{V}$, and R_D equal to 10kΩ, A_{VO} is $141.4\frac{V}{V}$ or 43.0dB.

3 Simulated Performance

To ensure specifications are met, the circuits created in the design section were simulated. All simulations were done using Micro−Cap 12 (64−bit), making use of the UMaine micro−cap parts library. Simulations were run to investigate the effect of input and output loading on the gain of the circuit.

3.1 Common Emitter Amplifier

Figure 3 shows the common emitter amplifier circuit as seen in Micro−Cap.

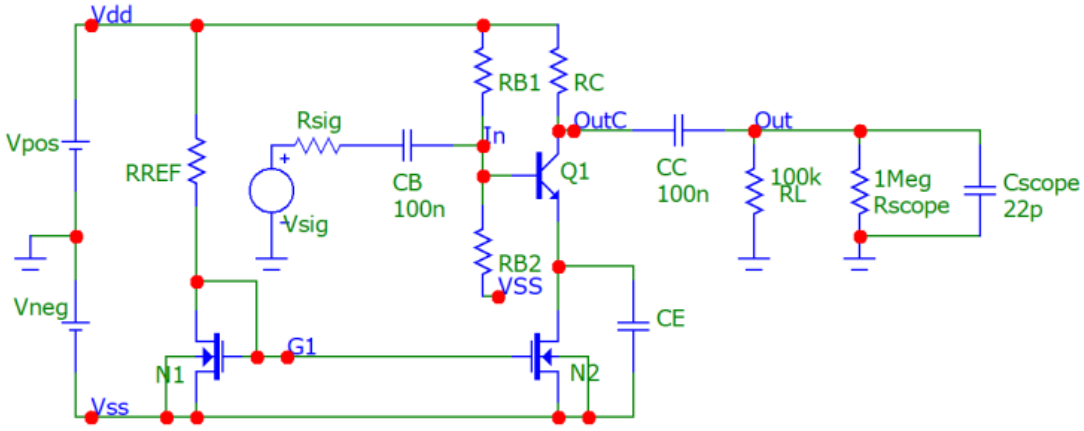

Fig. 3. Common emitter amplifier as seen in Micro−Cap.

Several simulations are run on the common emitter circuit. The first is a dynamic DC simulation to determine the terminal voltages of the 2N3904. Then, a series of AC simulations are run to investigate the unloaded voltage gain. Lastly, transient simulations are run to investigate limits on the input voltage amplitude.

3.1.1 Dynamic DC

A Dynamic DC simulation is used to investigate the DC operating point of a given circuit. No values are changed, instead the node voltages and currents are shown on top of the schematic. Figure 4 shows the results of the Dynamic DC simulation.

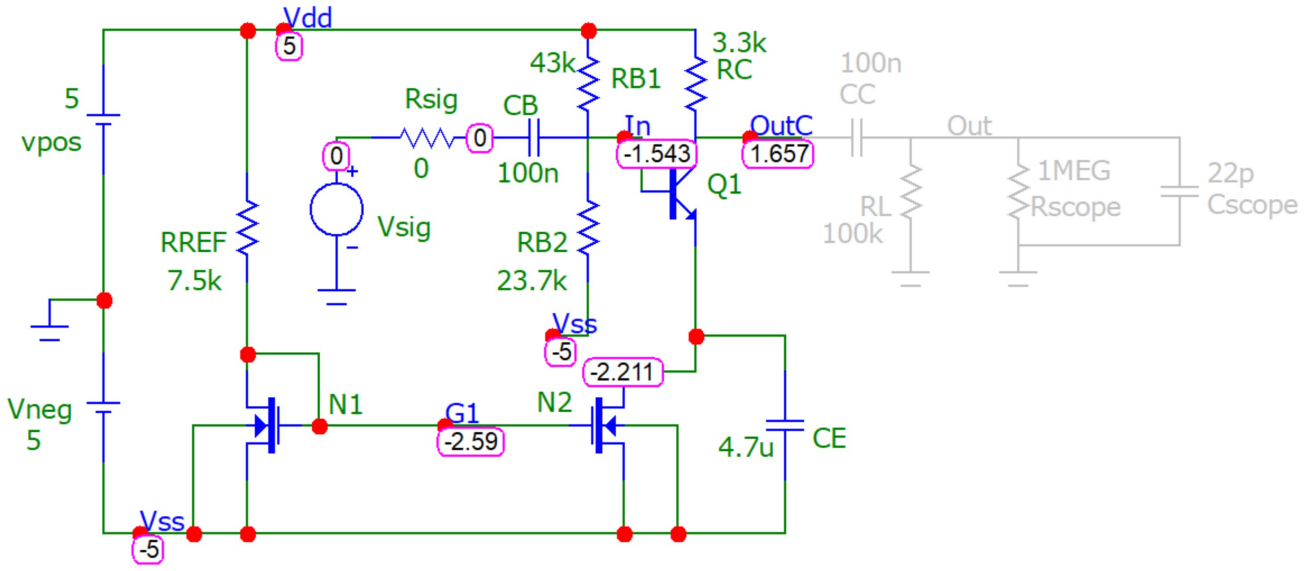

Fig. 4. Dynamic DC simulation of the common emitter circuit.

As can be seen, the input and output are unloaded to get accurate DC operating point values. The collector voltage V_C is equal to 1.657V. The base voltage V_B is -1.543V, meeting the specified value of 1.5V$\pm$0.3V. The emitter voltage V_E is -2.211V. The terminal voltages are tabulated in Table I.

3.1.2 Frequency Response

Frequency response simulations are run to investigate the gain of the amplifier circuit, as well as the phase shift. Figure 5 shows the results of the frequency response with no loading on the input or output.

V_B	V_C	V_E
-1.543	1.657	-2.211

TABLE I
Common emitter amplifier terminal voltages.

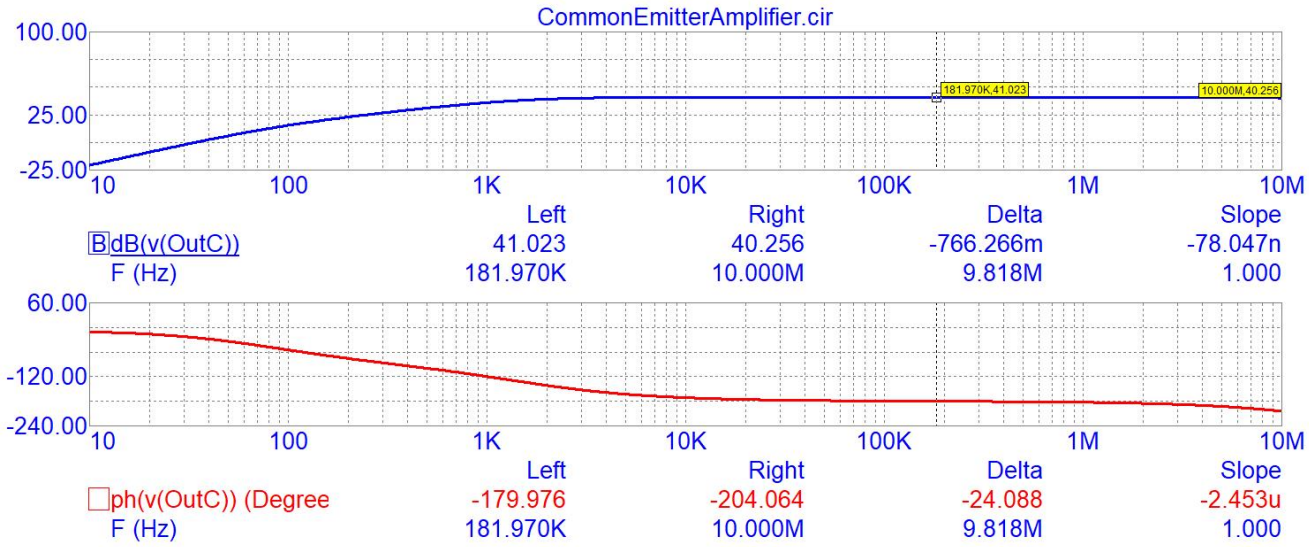

Fig. 5. Frequency response of the common emitter amplifier with no input or output loading.

As can be seen, the unloaded voltage gain reaches a peak of 41.023dB, meeting design specifications. The phase plot also looks as expected, showing at least three poles, due to the three capacitors in the circuit. Next, the signal resistance is changed to 50Ω and the load resistance R_L is stepped over the values 1kΩ, 10kΩ, and 100kΩ. Frequency response simulations are run again. Figure 6 shows the results of the frequency response with R_{SIG} equal to 50Ω and R_L equal to 1kΩ.

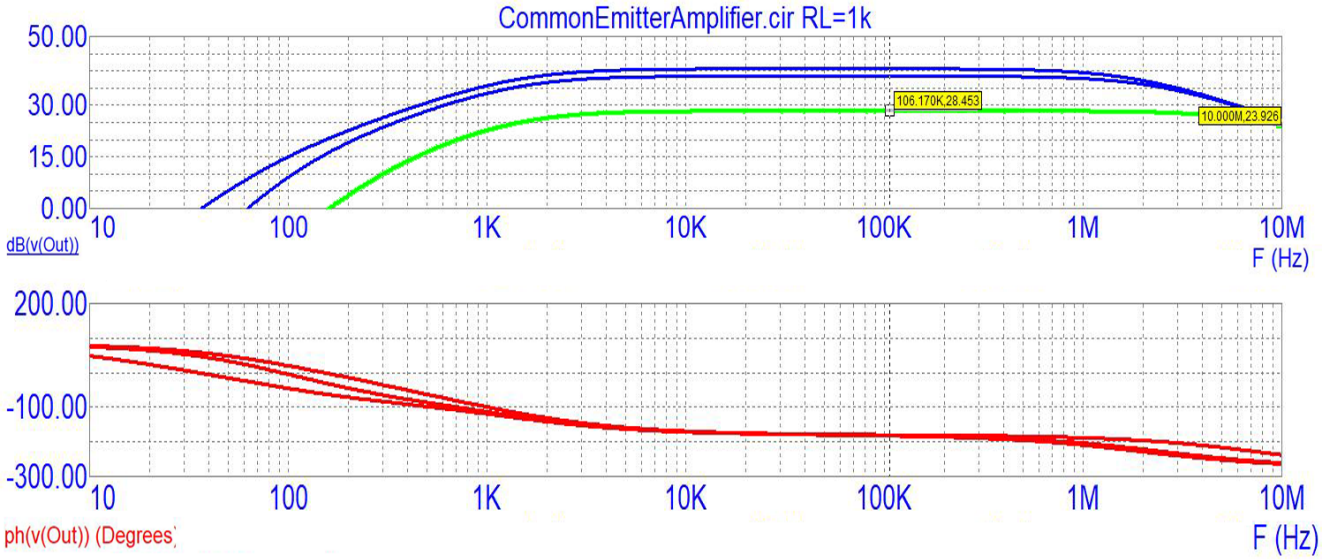

Fig. 6. Frequency response of the common emitter amplifier with R_{SIG} = 50Ω and R_L = 1kΩ.

Here, the peak gain is 28.453dB. This is significantly below expected, and can be explained by the load

resistance being comparable to the output resistance of 3161Ω. When this happens, the gain is reduced significantly due to the output loading of the circuit. The lower cutoff frequency is found to be 1.583kHz. This meets the required specification of being below 2kHz. Figure 7 shows the results of the frequency response with R_{SIG} equal to 50Ω and R_L equal to 10kΩ.

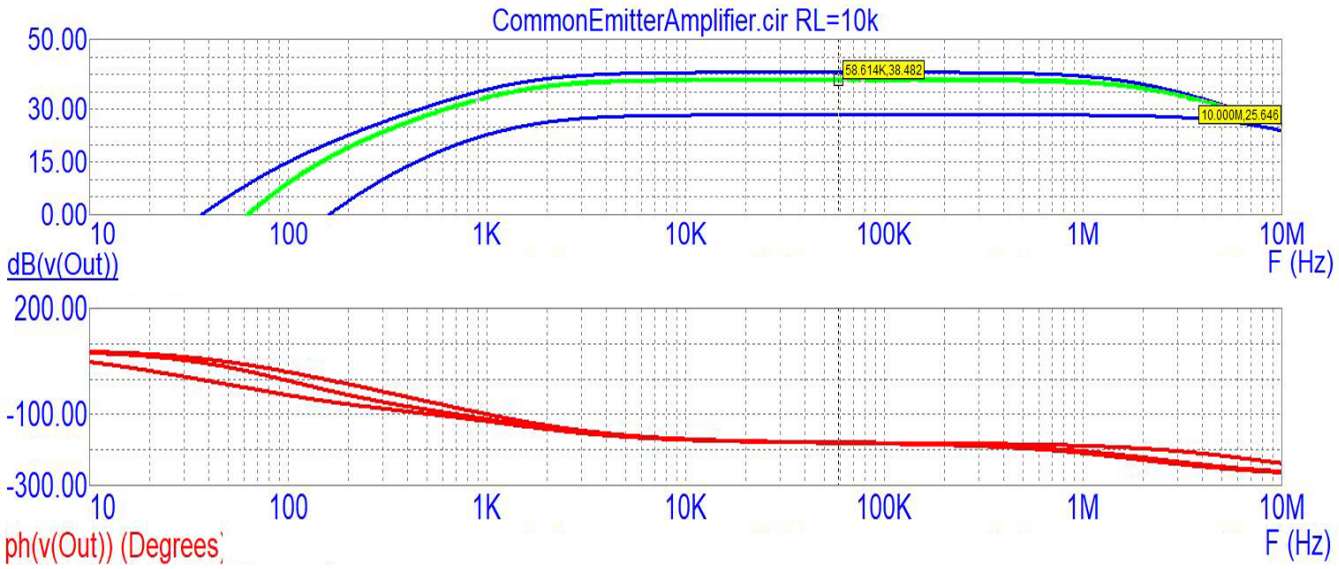

Fig. 7. Frequency response of the common emitter amplifier with R_{SIG} = 50Ω and R_L = 10kΩ.

As can be seen, the peak gain is 37.259dB. This more closely matches the unloaded gain, and this improvement can be explained by the load resistance being larger than the output resistance. Because of this, the gain is is still reduced but not as much as the 1kΩ case. The lower cutoff frequency is found to be 1.480kHz. This is slightly lower than before, and further meets the required specification of below 2kHz. Figure 8 shows the results of the frequency response with R_{SIG} equal to 50Ω and R_L equal to 100kΩ.

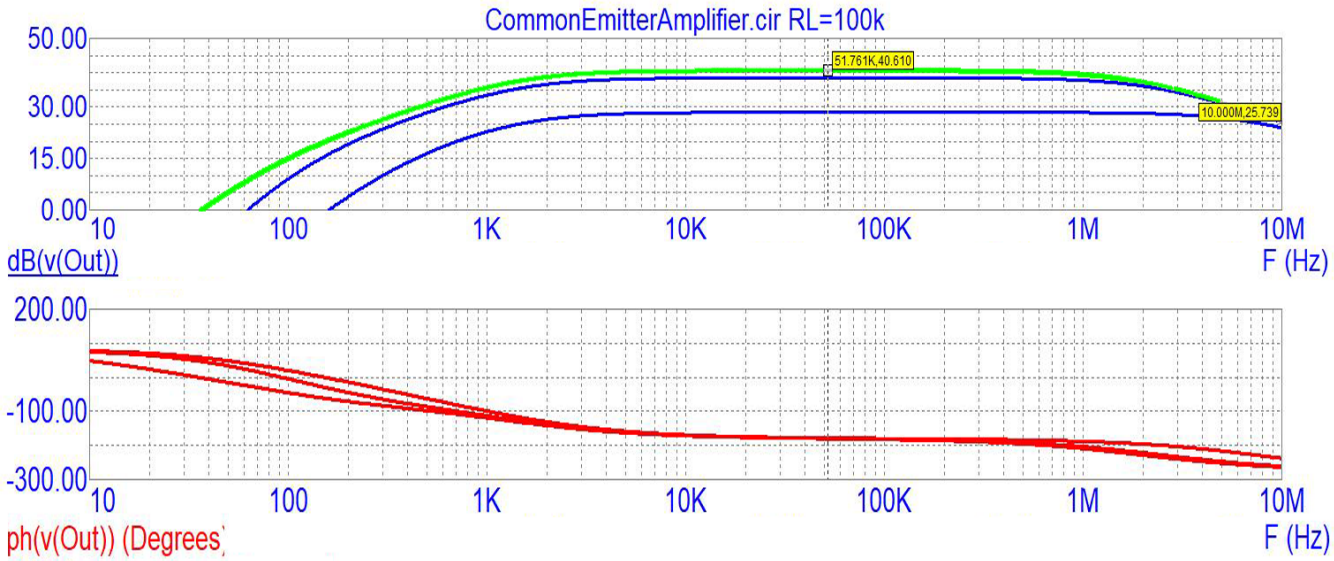

Fig. 8. Frequency response of the common emitter amplifier with R_{SIG} = 50Ω and R_L = 100kΩ.

Here, the peak gain is 40.610dB. This closely matches the unloaded gain, this improvement can be explained by the load resistance being an order of magnitude larger than the output resistance. Because of this, the gain is is barely reduced compared to the unloaded voltage gain. The lower cutoff frequency is found to be 1.461kHz. This is slightly lower than before, and even further meets the required specification of being below 2kHz. Clearly, the output loading of the circuit does not significantly impact the low cutoff frequency of the amplifier. This is because the capacitor C_E that is used to determine the low cutoff frequency only sees the smallest resistance. Lastly, the signal resistance R_{SIG} is changed to 2kΩ to investigate effects of input loading on the amplifier. Figure 9 shows the results of the frequency response with R_{SIG} equal to 2kΩ and R_L equal to 100kΩ.

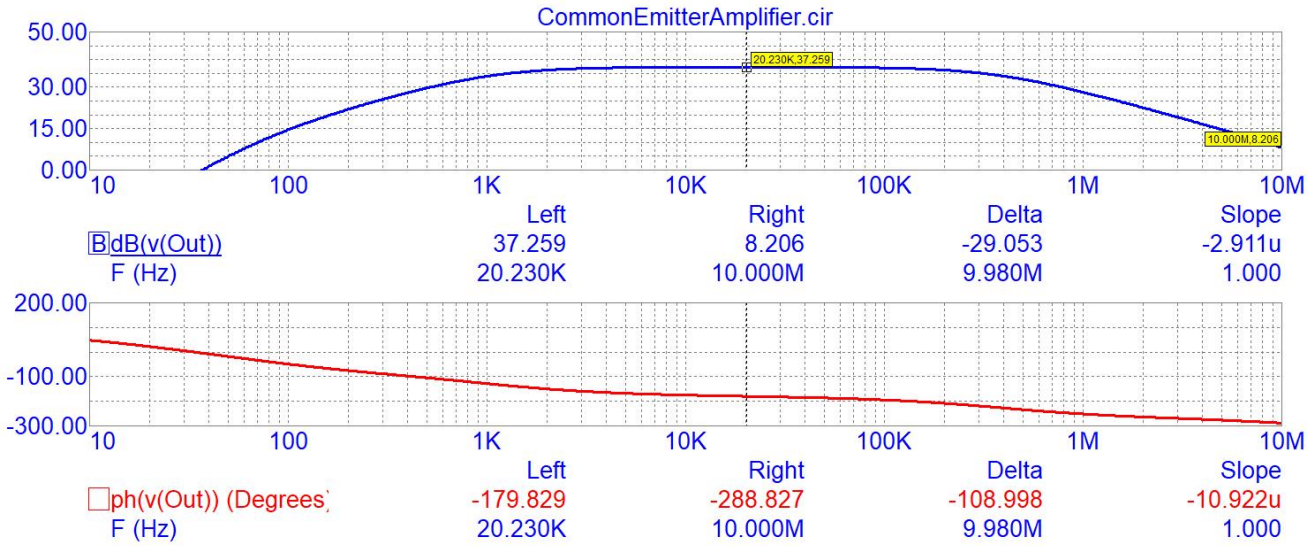

Fig. 9. Frequency response of the common emitter amplifier with R_{SIG} = 2kΩ and R_L = 100kΩ.

Here, the peak gain is 37.259dB. This is lower than the 50Ω case because the overall voltage gain includes impedance loading on the input of the circuit. With a signal resistance closer to the input resistance, the gain is reduced.

3.1.3 Transient Response

Two transient simulations are run on the circuit to investigate the maximum allowable input voltages. Figure 10 shows the transient simulation with a 10kHz 10mVp signal.

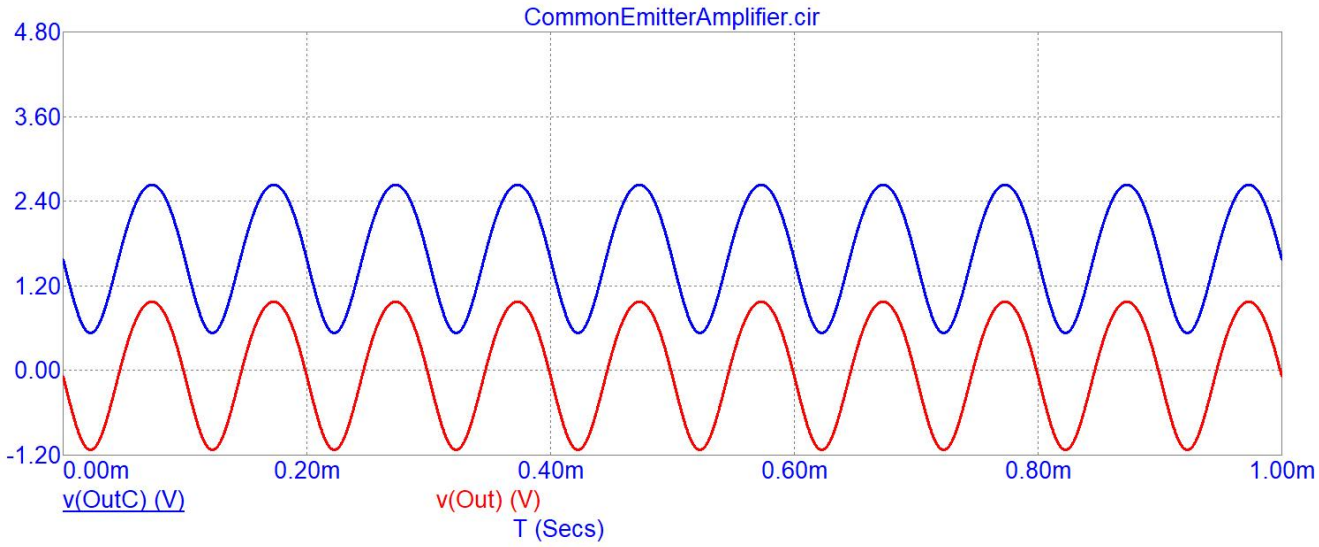

Fig. 10. Transient simulation of the common emitter amplifier with a 10kHz 10mVp signal

As can be seen, the output signal is amplified as expected. The blue curve shows the output taken before the collector capacitor, and the red shows the output after the capacitor. The blue curve has a significant DC offset from the terminal voltages, and the red does not. This shows the collector capacitor successfully providing DC decoupling of the circuit. Additionally, the output is not clipping, it is a full sine wave. Figure 11 shows the transient simulation with a 10kHz 100mVp signal.

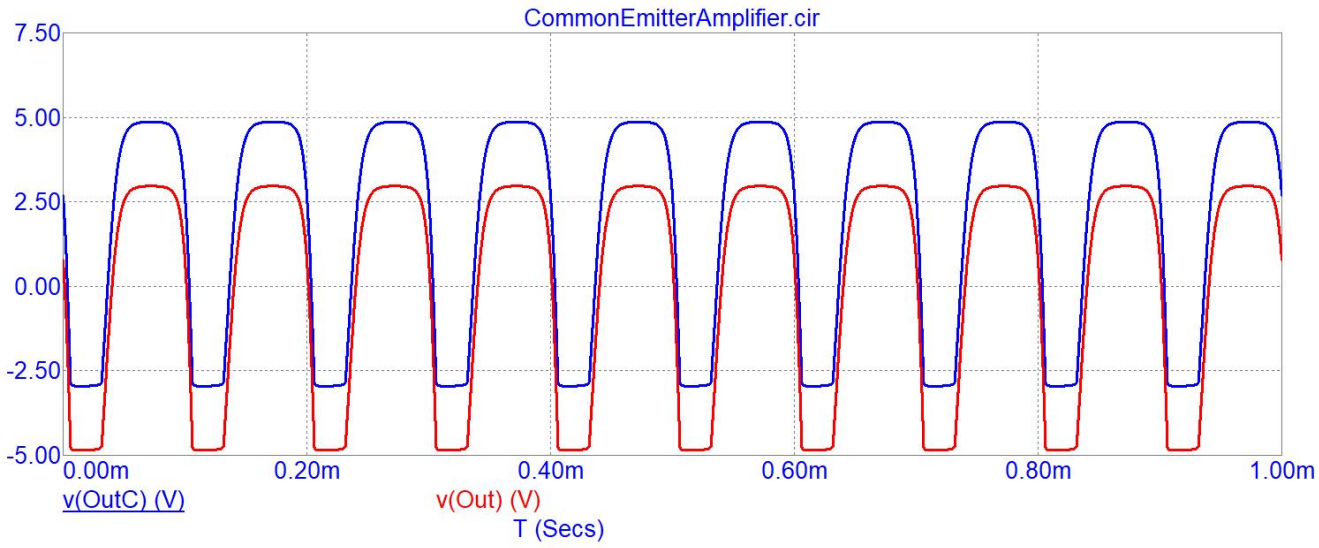

Fig. 11. Transient simulation of the common emitter amplifier with a 10kHz 100mVp signal

As can be seen, the output signal is still amplified, but the output is cutoff at the top and bottom. This

is because the signal is amplified too much, and exceeds the supply voltages of ±5V. Clearly, the input voltage is too high. The maximum allowable input voltage is determined to be 25mVp, at this level, the output voltage is not saturated on either end. The DC offset can still be seen on the blue curve, as explained above. Ultimately, the common emitter amplifier performs as expected from calculations. The unloaded gain meets the specification of being above 40dB, and the lower cutoff frequency is well below the specified limit of 1kHz.

3.2 Common Gate Amplifier

Figure 12 shows the common gate amplifier circuit as seen in Micro−Cap.

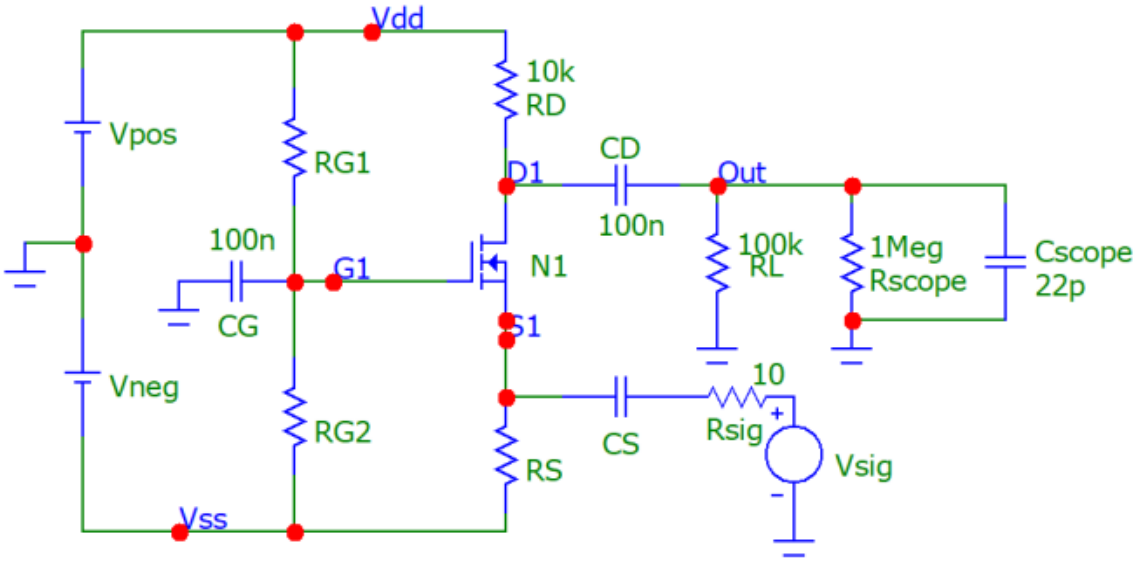

Fig. 12. Common gate amplifier as seen in Micro−Cap.

Several simulations are run on the common gate circuit. The first is a dynamic DC simulation to determine the terminal voltages of the 2N7000. Then, a series of frequency response simulations are run to investigate the voltage gain. Lastly, transient simulations are run to investigate limits on the input voltage amplitude.

3.2.1 Dynamic DC

Figure 13 shows the results of the Dynamic DC simulation.

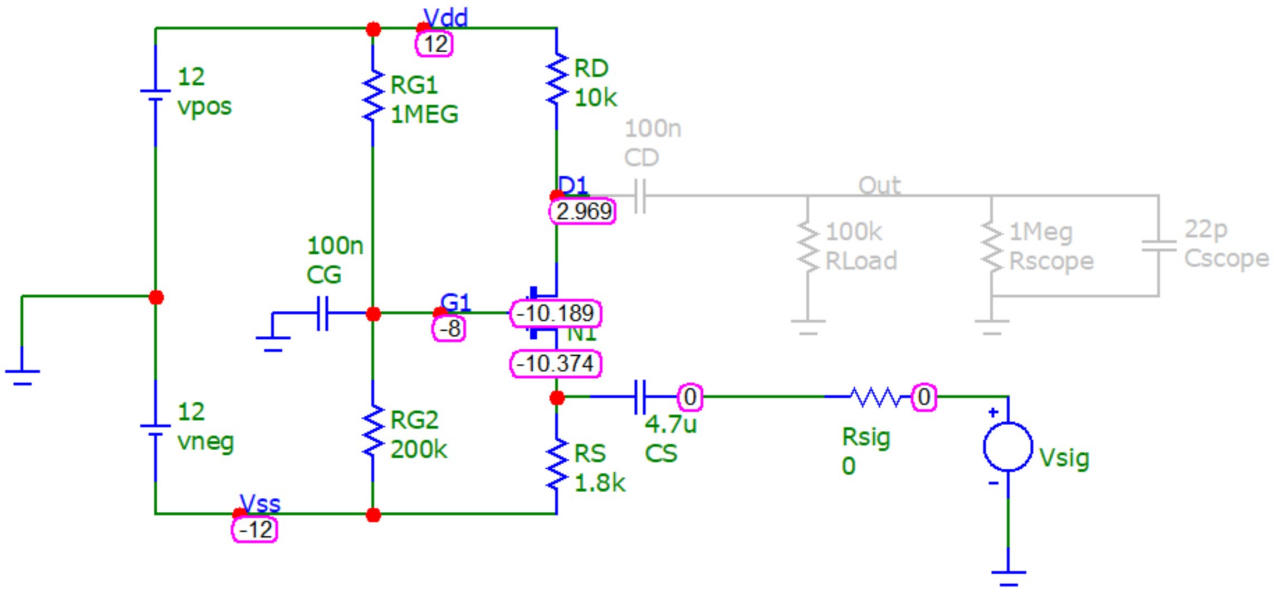

Fig. 13. Dynamic DC simulation of the common gate circuit.

As can be seen, the input and output are unloaded to get accurate DC operating point values. The gate voltage V_G is equal to -8V. The drain voltage V_D is 2.969V. The source voltage V_S is -10.374V. These values match the biased MOSFET circuit built in Experiment 4 as expected. The terminal voltages are tabulated in Table II.

3.2.2 Frequency Response

Frequency response simulations are run to investigate the gain of the amplifier circuit, as well as the phase shift. Figure 14 shows the results of the frequency response with no loading on the input or output.

V_G	V_S	V_D
-8	-10.374	2.969

TABLE II
Common emitter amplifier terminal voltages.

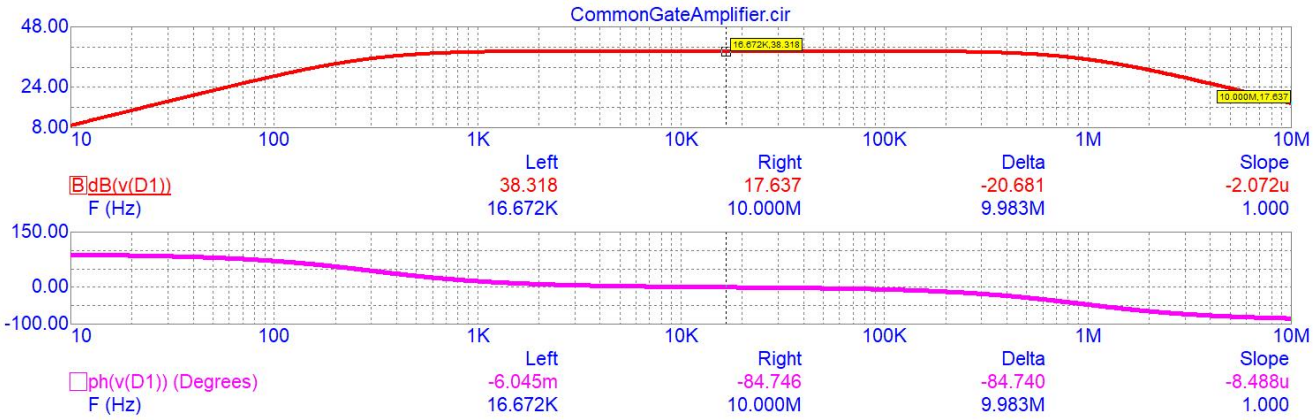

Fig. 14. Frequency response of the common gate amplifier with no input or output loading.

As can be seen, the unloaded voltage gain reaches a peak of 38.318dB, there was no specification on this gain, but it is slightly lower than expected. This is likely due to variations in the simulation model compared to values used in calculations. The phase plot looks as expected. Next, the signal resistance is kept at 0Ω and the load resistance R_L is stepped over the values 1kΩ, 10kΩ, and 100kΩ. Frequency response simulations are run again. Figure 15 shows the results of the frequency response with R_{SIG} equal to 0Ω and R_L equal to 1kΩ.

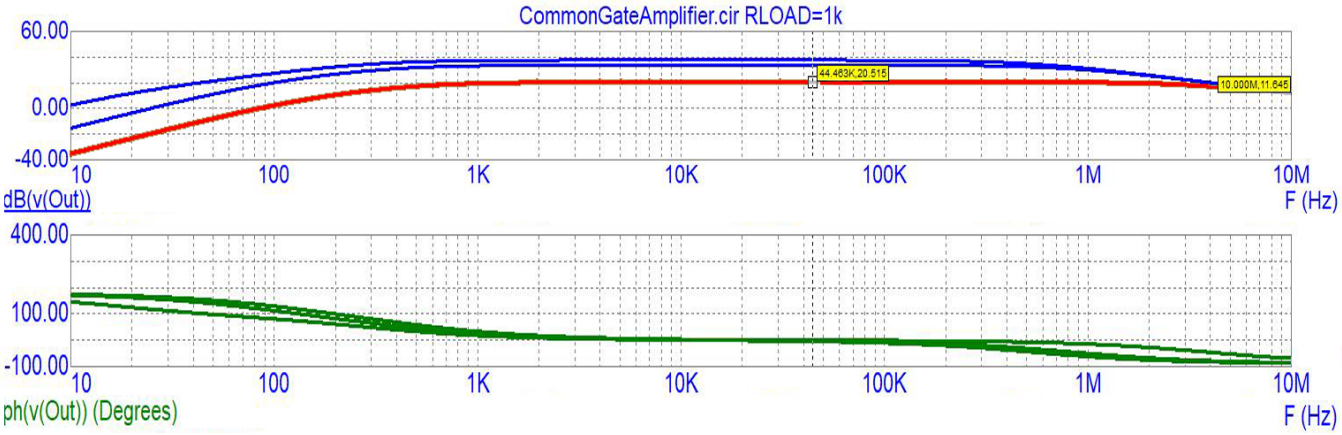

Fig. 15. Frequency response of the common gate amplifier with R_{SIG} = 0Ω and R_L = 1kΩ.

Here, the peak gain is 20.515dB. This is significantly below expected, and can be explained the same as with the common emitter amplifier. The load resistance is comparable to the output resistance of 3.161kΩ, thus significantly reducing the gain due to the output loading of the circuit. The lower cutoff frequency is found to be 525Hz. This meets the required specification of below 1kHz. Figure 16 shows the results of the frequency response with R_{SIG} equal to 0Ω and R_L equal to 10kΩ.

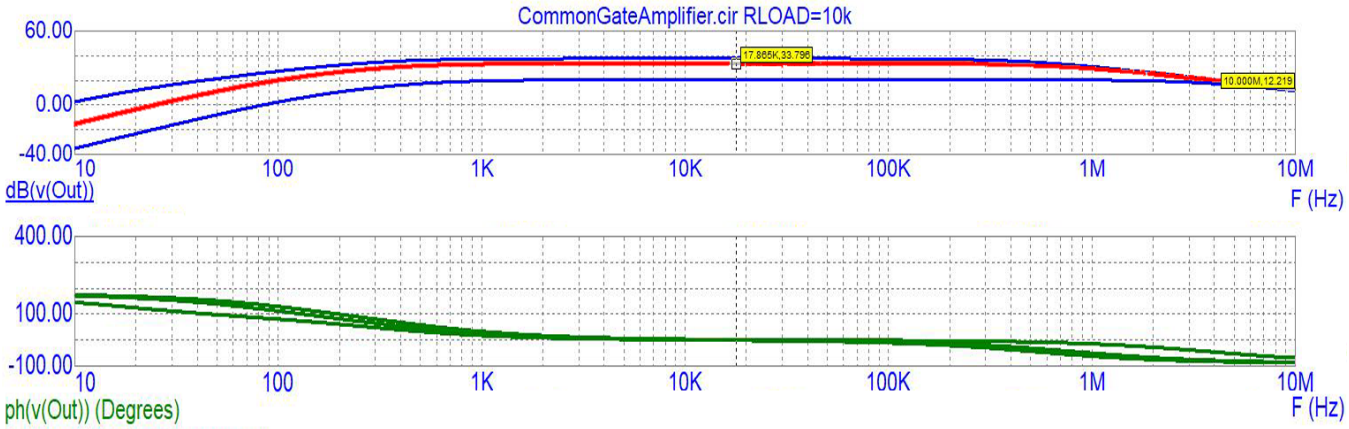

Fig. 16. Frequency response of the common emitter amplifier with R_{SIG} = 0Ω and R_L = 10kΩ.

Here, the peak gain is 33.796dB. As with the common emitter, this more closely matches the unloaded gain. This improvement can be explained by the load resistance being larger than the output resistance, reducing the gain, but not as much as the 1kΩ case. The lower cutoff frequency is found to be 386Hz. This is lower than before, and further meets the required specification of below 1kHz. Figure 17 shows the results of the frequency response with R_{SIG} equal to 0Ω and R_L equal to 100kΩ.

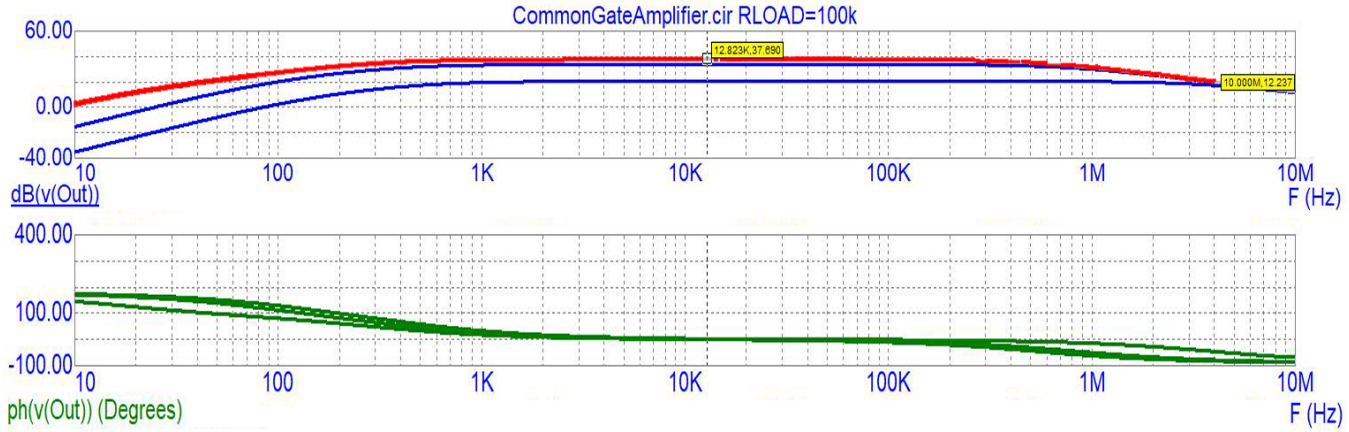

Fig. 17. Frequency response of the common emitter amplifier with R_{SIG} = 0Ω and R_L = 100kΩ.

As can be seen, the peak gain is 37.690dB. This is much closer to the unloaded gain, because the load resistor is an order of magnitude larger than the output resistance. As a result, the gain is barely affected. The lower cutoff frequency is found to be 308Hz. This is again lower than before, and even further meets the required specification of below 2kHz.

3.2.3 Transient Response

Two transient simulations are run on the circuit to investigate the maximum allowable input voltages. The common gate amplifier can accept a higher input voltage than the common emitter amplifier, this will be seen in the following simulations. Figure 18 shows the transient simulation with a 10kHz 100mVp signal.

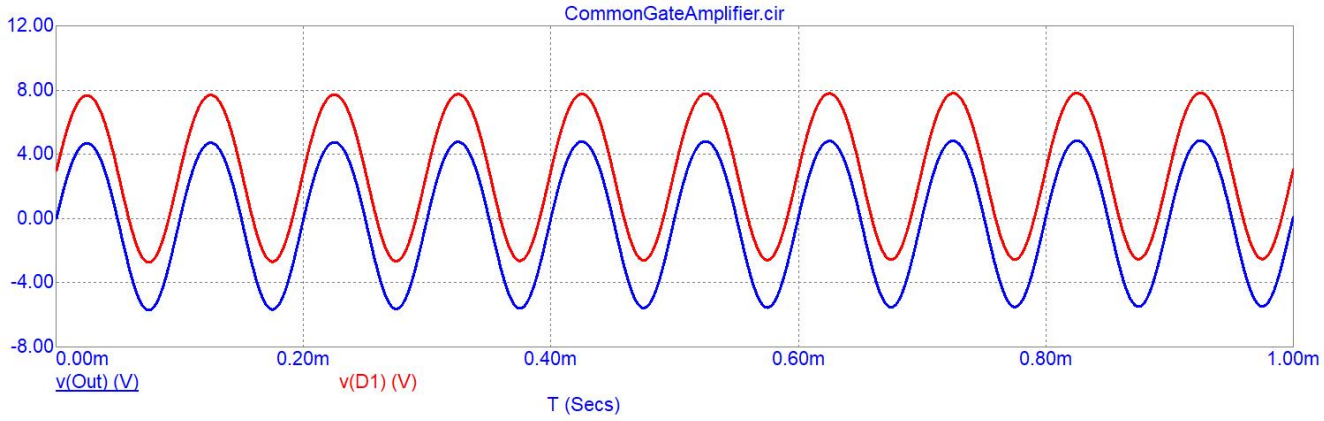

Fig. 18. Transient simulation of the common gate amplifier with a 10kHz 100mVp signal

As can be seen, the output signal is amplified as expected. The blue curve shows the output taken before the drain capacitor, and the red shows the output after the capacitor. The blue curve has a significant DC offset from the terminal voltages, and the red does not. As with the common emitter amplifier, this shows the collector capacitor successfully providing DC decoupling of the circuit. Additionally, the output is not clipping, it is a full sin wave.

Figure 19 shows the transient simulation with a 10kHz 200mVp signal.

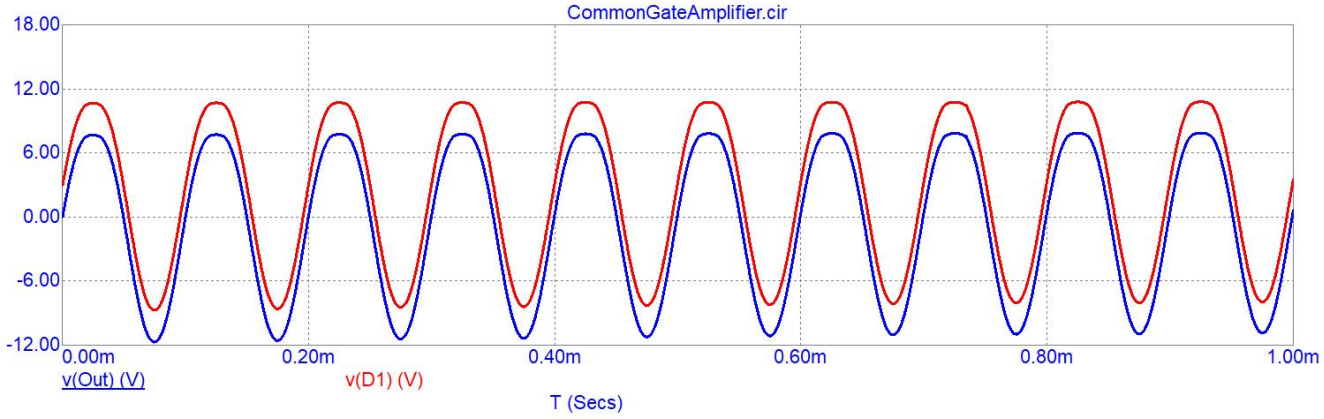

Fig. 19. Transient simulation of the common gate amplifier with a 10kHz 200mVp signal

As can be seen, the output signal is still amplified, but the output is cutoff at the top and bottom. As with the common emitter amplifier, this is because the signal is amplified too much, and exceeds the supply voltages of $\pm$12V. Clearly, the input voltage is too high. The maximum allowable input voltage is determined to be 180mVp. At this level, the output voltage is not saturated on either end. The DC offset can still be seen on the blue curve, as explained above. Ultimately, the common gate amplifier performs as expected from calculations. The lower cutoff frequency is well below the specified limit of 1kHz, being below 550Hz for each load simulated..

4 Experimental Implementation

All measurements are taken using the Digilent Analog Discovery 2 (DAD2) in conjunction with Digilent's WaveForms software. Component values are measured with a Neotek NT8233D Pro multimeter. The voltage gain for both amplifiers is measured, as well as the current for the common emitter amplifier.

4.1 Common Emitter Amplifier

Figure 20 shows the final schematic for the Common Emitter Amplifier. Multiple measurements were taken, where R_L is $100k\Omega$ and $1k\Omega$. Measurements for this circtuit were taken with both the Neotek multimeter as well as the DAD2.

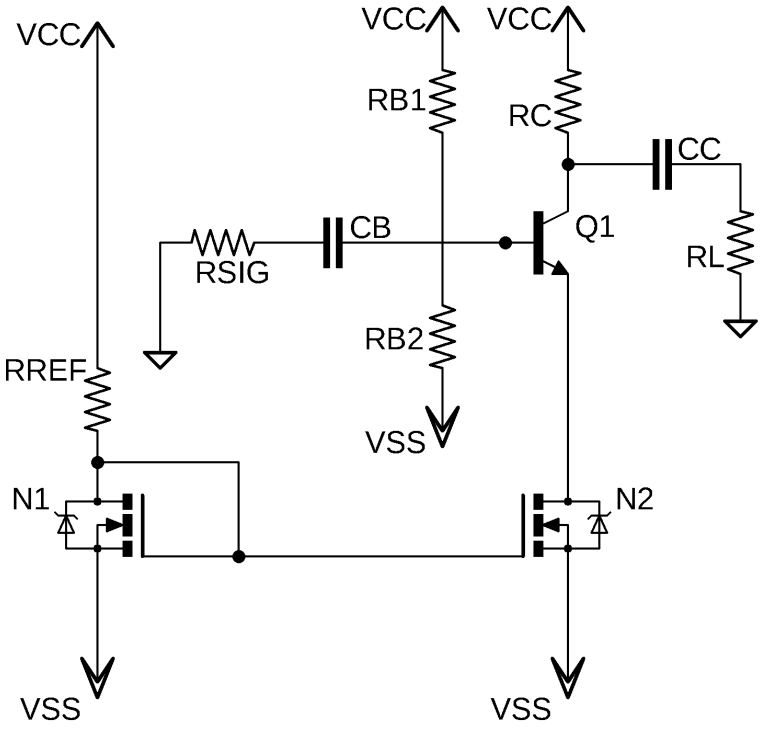

Fig. 20. Final common Emitter amplifier circuit schematic.

This circuit is built using a 2N3904 from ON Semiconductor. In all measurements, RSIG is practically zero, because the DAD2 breakout board was not used, therefore there is little to no signal source impedance from the DAD2. For this circuit, the input as defined as the base terminal of the BJT, and the output is defined as the collector terminal of the BJT.

TABLE III
Measured Components of the common emitter amplifier

Component	Nominal Value (Ω)	Measured Value (Ω)
R_{B1}	43.3k	43.3
R_{B2}	23.7k	34.1
R_C	3.3k	3.26k
R_L	100k	99.8k
R_L	1k	998
C_E	$4.7\mu F$	—

4.1.1 Current Measurements

Current is measured through both the MOSFET of the current mirror and the BJT of the amplifier. Current is measured at two different loads, where $R_L = 1k\Omega$ and $R_L = 100k\Omega$. The measurement is taken by using the current measurement functionality of a multimeter at the junction of R_C and the emitter of the BJT. The positive lead of the multimeter was connected R_C and the negative lead is connected to the emitter of the BJT.

TABLE IV
Measured Components of the common emitter amplifier

Component	1k Load	100k Load
N_1	1.00mA	1.00mA
Q_1	1.01mA	0.95mA

4.1.2 Frequency Response

The frequency response is measured at two different load resistances, $R_L = 1k\Omega$ and $R_L = 100k\Omega$. The DAD2's network analyzer tool is used, to sweep from 10Hz to 1MHz with an amplitude of 100mV.

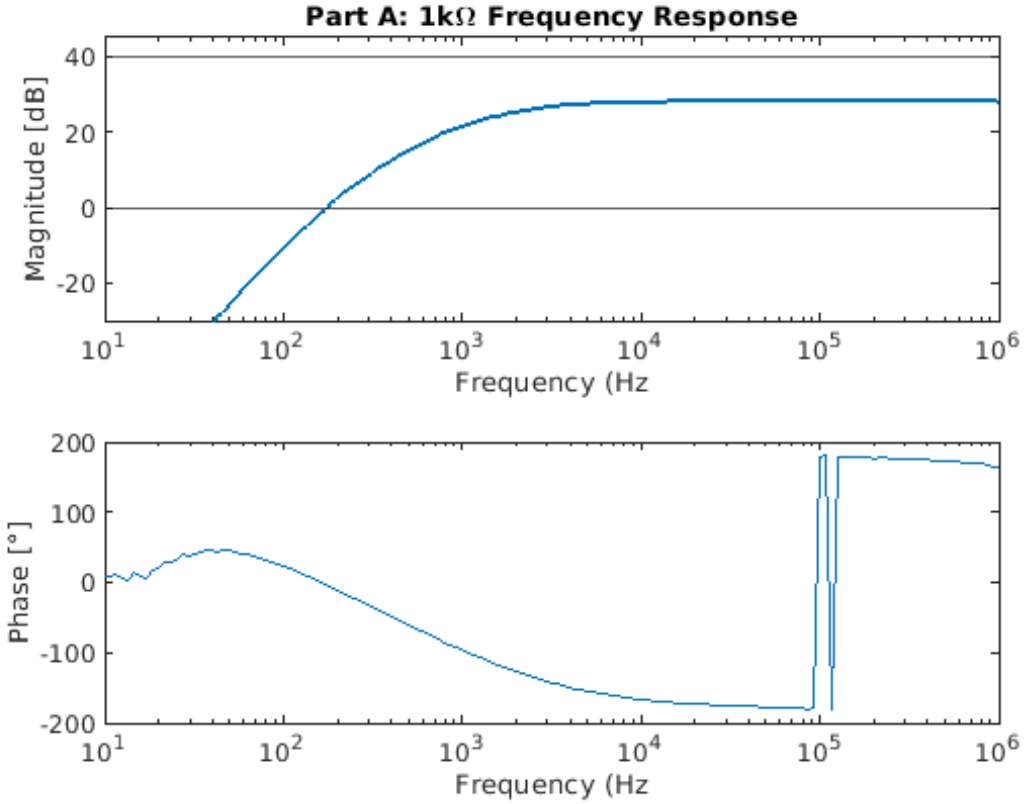

Fig. 21. Frequency response of the common emitter amplifier with $R_L = 1k\Omega$.

With a $1k\Omega$ load, the common emitter amplifier has a peak magnitude of 28.5 dB. This closely matches the simulated performance of 28.453dB as discussed in section 3, simulations. With a load of 1kΩ, the lower cutoff frequency is 1.71kHz.

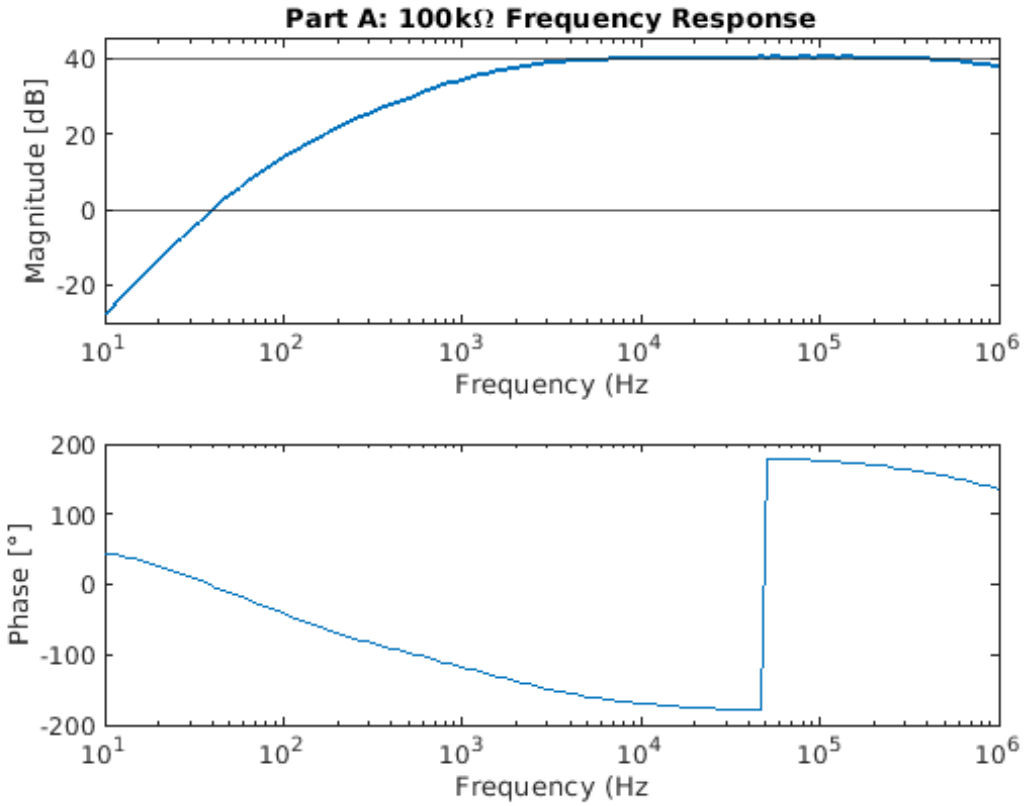

Fig. 22. Frequency response of the common emitter amplifier with $R_L = 100k\Omega$.

As can be seen, with a $100k\Omega$ load, the common emitter amplifier has a 40.75 dB gain, which matches the simulated value of 40.61 dB. The lower cutoff frequency with a 100kΩ load is at 1.58kHz.

4.1.3 Transient Response

The transient response of the common emitter amplifier is measured with the same load resistances as the frequency response, $1k\Omega$ and $100k\Omega$. The DAD2 is used to generate a 10kHz sine wave with voltages of 100mV and 10mV. Both channels of the DAD2's oscilloscope are used to measure both the voltage in and the voltage out.

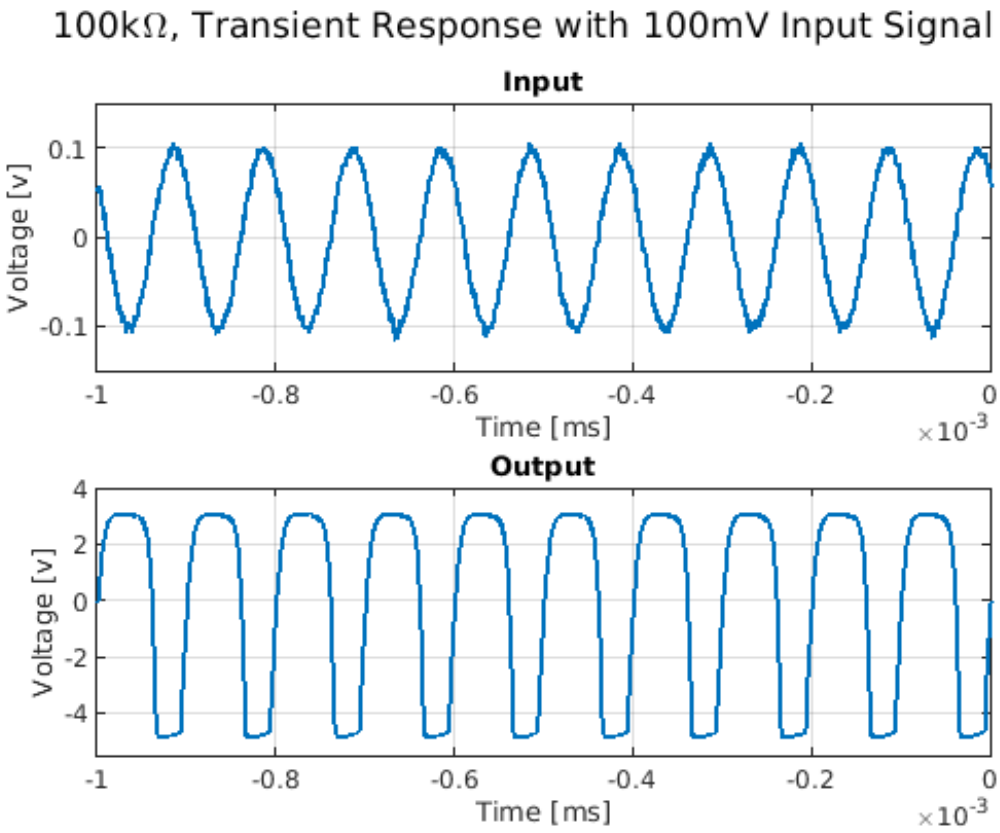

Fig. 23. Common emitter amplifier transient analysis with 100mV input signal.

As can be seen if Figure 23, with a 100k load and a 100mV input signal the output signal is clipping on the upper and lower regions of the signal. The output signal has a voltage swing of 7.79V, as the positive side of the signal saturates at approximately 3V and the negative side saturates and approximately −4.79V.

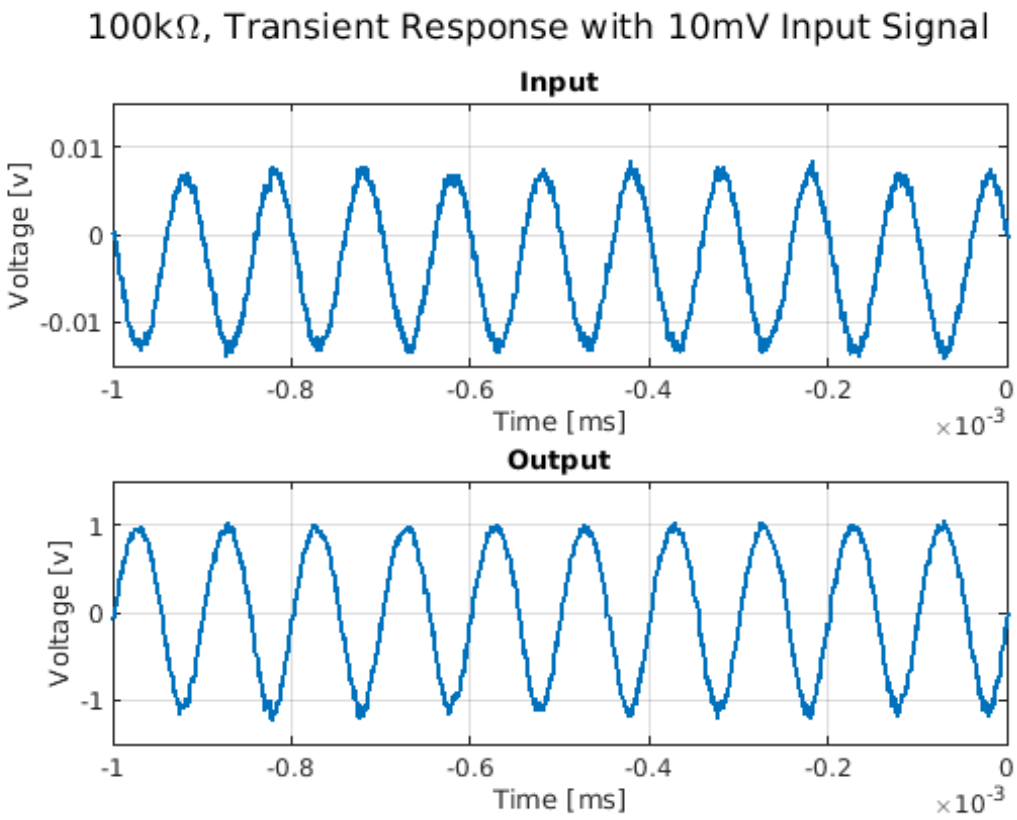

Fig. 24. Common emitter amplifier transient analysis with 10mvV input signal and $R_L = 100k\Omega$.

When the input voltage is changed from a sinusoid with 100mV amplitude to a sinusoid with a 10mV amplitude, the output signal has an amplitude of 1V and has no clipping on the peaks and troughs of the signal as it is not saturating the transistor.

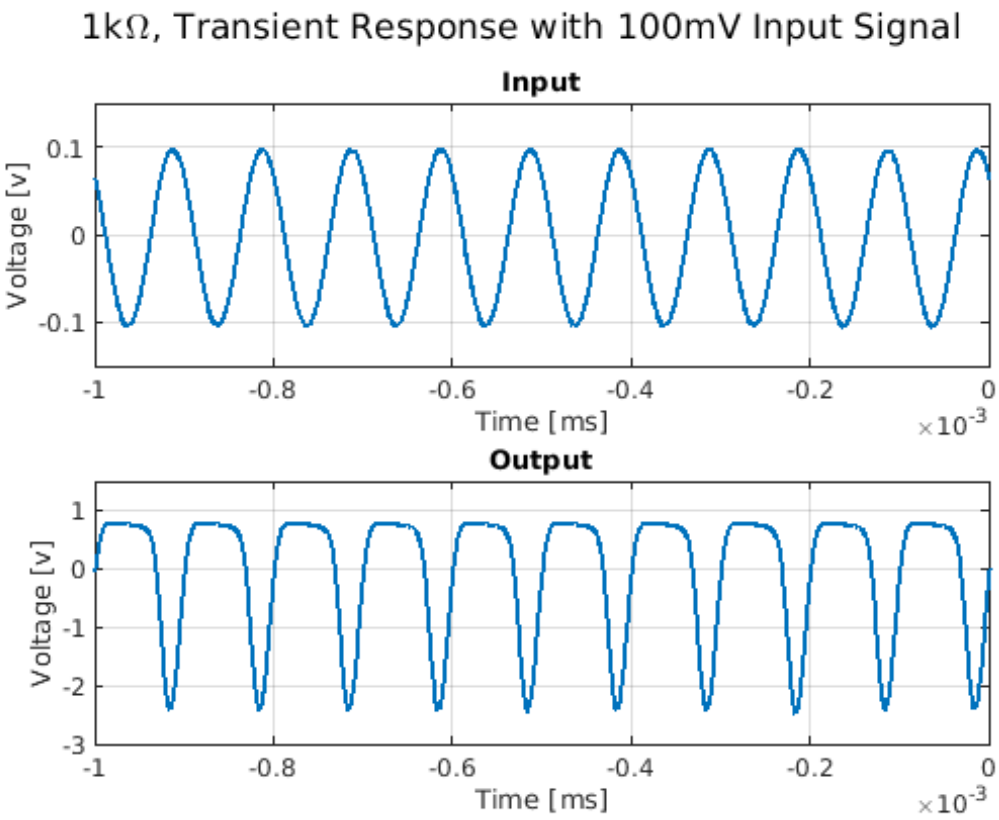

Fig. 25. Commen emitter amplifier transient analysis with 100mV input signal and $R_L = 1k\Omega$.

For the next two measurements, the load resistance was changed from $100k\Omega$ to $1k\Omega$. As seen in figure 25, the output signal has a similar shape to that of the output signal with a $100k\Omega$ load (Figure 23, but is saturating at 790mV and -2.35V.

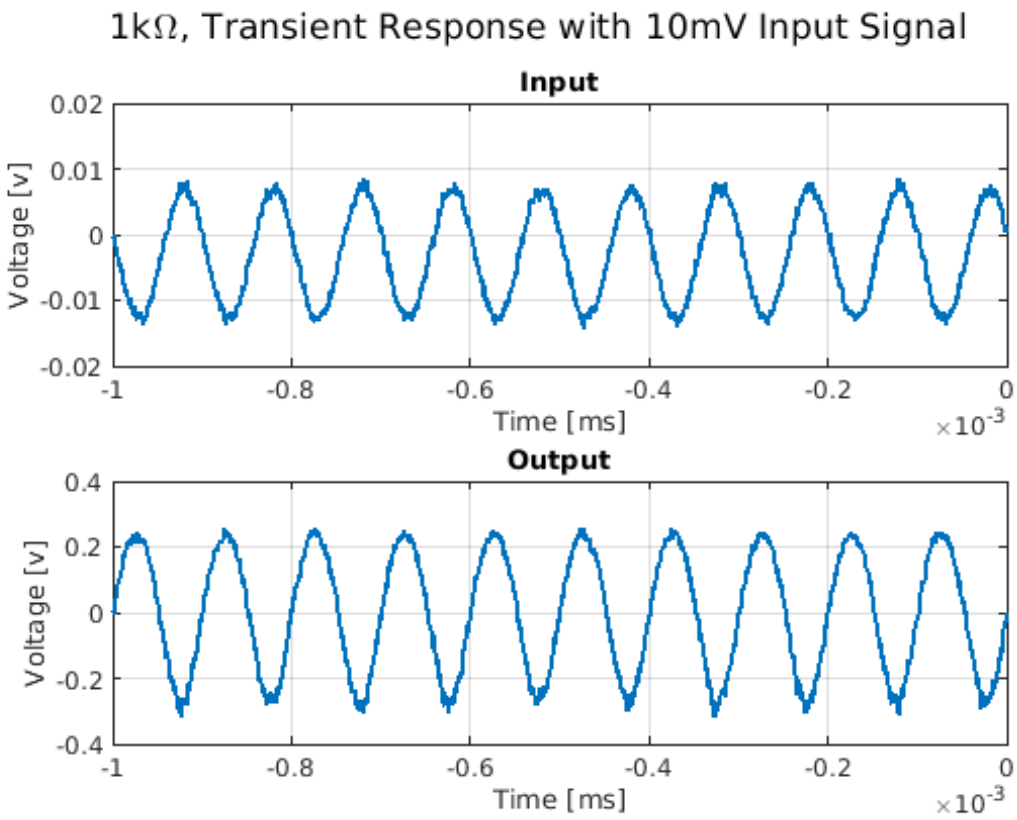

Fig. 26. Caption

Figure 26 shows the transient analysis of the common emitter amplifier when the input signal is changed to a 10mV sine wave, which outputs a 240mV sine wave without clipping.

4.2 Common Gate Amplifier

Figure 27 shows the common gate amplifier schematic.

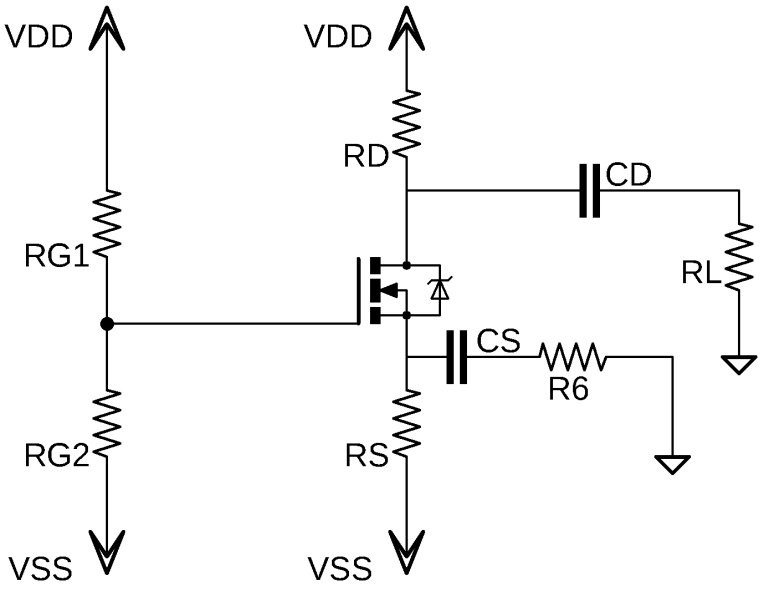

Fig. 27. Final common gate amplifier circuit schematic.

The circuit is built using a 2N7000 MOSFET. In all measurements, R_{SIG} is practically zero, because the DAD2 breakout board was not used, therefore there is little to no signal source impedance from the DAD2. For this circuit, the input is defined as the gate terminal of the MOSFET, and the output is defined as the drain terminal of the MOSFET. Components are measured to find their exact values. Table V shows the nominal and measured values for each component.

TABLE V
Measured Components of the common gate amplifier

Component	Nominal Value (Ω)	Measured Value (Ω)
R_{G1}	1M	1.003M
R_{G2}	200k	199k
R_D	10k	10.03k
R_S	1.8k	1.776k
R_L	100k	99.8k
R_L	1k	998

4.2.1 Frequency Response

The frequency response of the common gate amplifier is measured twice− once with the load resistor equal to 1kΩ and again with the load resistor changed to 100kΩ. In both cases, the signal supplied is a 10kHz 100mVp signal. Figure 28 shows the results of the frequency response with R_L equal to 1kΩ.

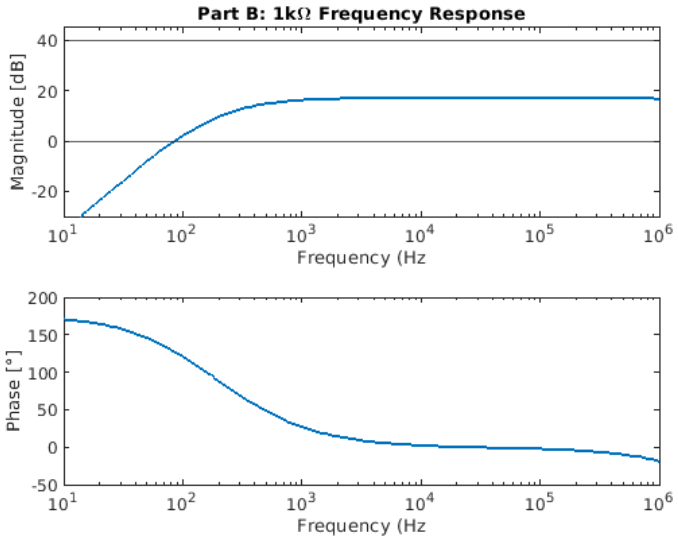

Fig. 28. Frequency response of the common gate amplifier with R_L = 1kΩ.

As can be seen, the peak gain of this configuration is 17.43dB. This is lower than the expected value of 20.515dB, and can likely be explained by unaccounted for resistances on the input and output. In $\frac{V}{V}$ this difference is only $1.4\frac{V}{V}$, not significantly impacting circuit performance. The lower cutoff frequency is 424Hz, which is again lower than the expected 525Hz, but it is still within the specified range of less than 1kHz. Figure 29 shows the results of the frequency response with R_L equal to 100kΩ.

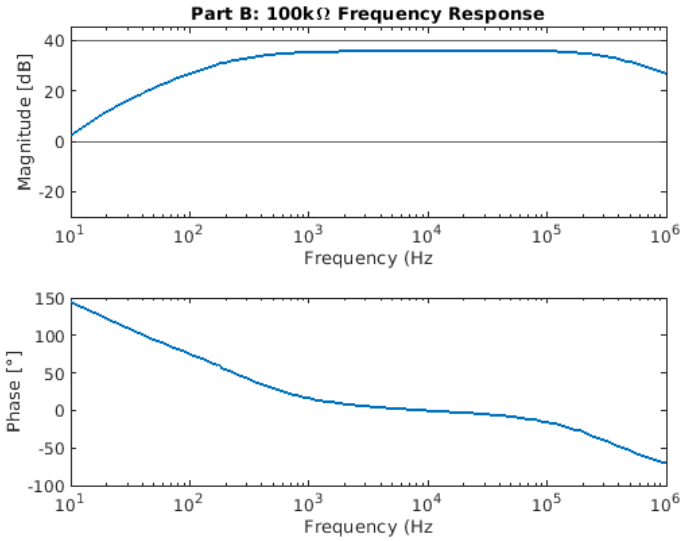

Fig. 29. Frequency response of the common gate amplifier with R_L = 100kΩ.

As can be seen, the peak gain of this configuration is 36.3dB. This is still lower than the expected value

of 37.690, but not as much as the 1kΩ case. This difference can likely be explained by tolerance values of the components, as well as parasitic input loading. The lower cutoff frequency is 298.1Hz , only slightly lower than the expected 308Hz. This measurement also matches specifications of being below 1kHz.

4.2.2 Transient Response

Three transient measurements were taken on the common gate amplifier. The first two are run with the input signal being a 100mVp 10kHz sine wave. The load resistor for the first two measurements is changed from 1kΩ to 100kΩ to investigate the effects of output loading. In the third measurement, the signal amplitude is reduced to 10mV, and the load resistor is kept at 100kΩ. Figure 30 shows the results of the transient measurement with a 100mVp signal and 100kΩ load resistor.

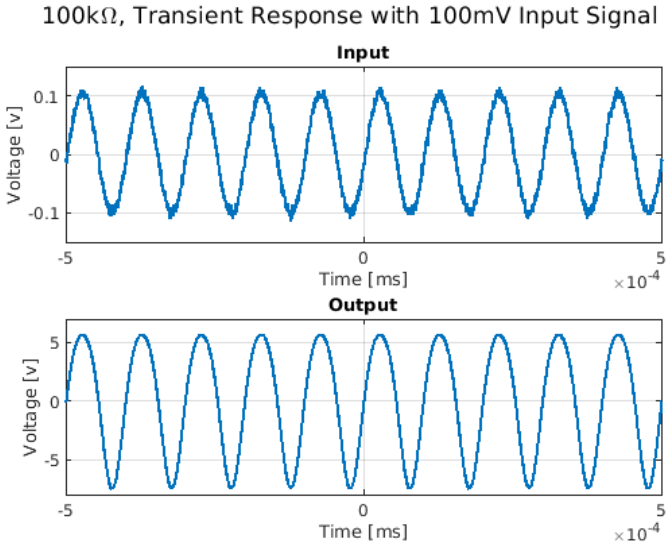

Fig. 30. Transient response of the common gate amplifier with R_L = 100kΩ and a 100mVp signal.

Here, the input signal is clearly amplified. The top signal shows the input signal taken from the waveform generator. The bottom signal is the output taken across the load resistor. The peak to peak voltage of the input signal is 230mV, with the output being 13V peak to peak. The output waveform is asymmetrical, as seen in simulations. Figure 31 shows the results of the transient measurement with a 100mVp signal and 1kΩ load resistor.

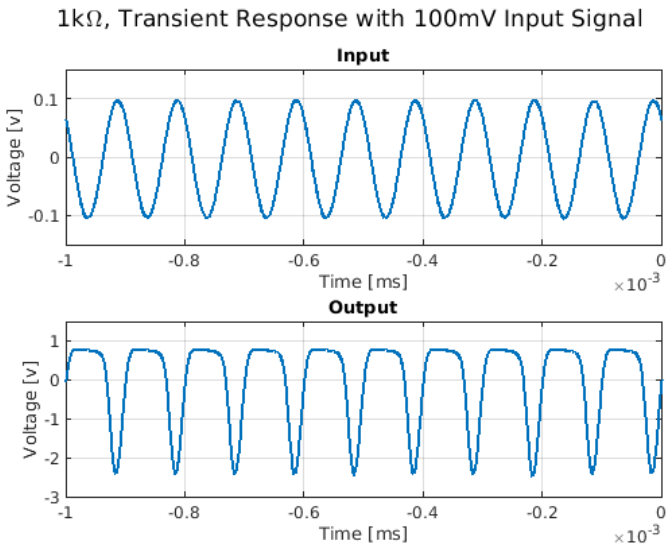

Fig. 31. Transient response of the common gate amplifier with R_L = 1kΩ and a 100mVp signal.

As can be seen, the signal is again amplified. The peak to peak voltage of the input signal is 205mV, and the output peak to peak voltage is 1.5403V. As expected, with the smaller load resistor, the amplification is lower than expected. As with the 100kΩ case, the output signal is asymmetrical. Ultimately, the circuit performs as expected, and properly amplifies AC signals applied to the input.

5 Discussion

Overall, each circuit works as expected, amplifying AC signals applied at their inputs. For the common emitter, the expected gain is 40dB with an appropriate load (e.g. 100kΩ). With a load $100k\Omega$, the peak gain was 40.76dB, which is a 1.9% error, this can be attributed to resistor tolerances. With a load of $1k\Omega$, the gain is only 28.5dB. With a load of $1k\Omega$ a 28.7% error from the ideal gain, this error makes sense when you take into account the output resistance of the amplifier. When compared to the simulated performance (which has a gain of 28.45dB) it is only an error of 0.17%. The common emitter is designed to have a lower cutoff frequency of 2kHz, which is met by all simulations and measurements. When the load is 1kΩ, the simulated cutoff frequency was 1.583kHz and the measured was 1.71kHz which is an error of 8.02%. When the load is 100kΩ, the simulated cutoff was 1.461kHz and the measured was 1.58kHz which is an error of 8.15%. The cutoff frequency is influenced by the capacitor C_E, which is only a 10% tolerance capacitor. Table VI shows a comparison of the various measurements at different stages of the experiment.

Measurement	Design	Simulation	Measurements
Ideal Voltage Gain (dB)	40	—	—
Unloaded Voltage Gain (dB)	40	41.023	—
1kΩ Voltage gain (dB)	—	28.453	28.5
100kΩ Voltage Gain (dB)	—	40.610	40.75
1kΩ f_LO (kHz)	<2	1.583	1.71
100kΩ f_LO (kHz)	<2	1.461	1.58

TABLE VI
Comparison of the common emitter amplifier voltage gain for each stage of the experiment.

The common gate amplifier also works as expected, especially with a 100kΩ load. The gain with a 1kΩ load was moderately far from it's expected value. The gain was measured to be 17.43dB, versus a simulated value of 20.515dB. This is a 16% error that can likely be explained by parasitic input loading on the circuit. The circuit was simulated with R_{SIG} equal to zero, as expected from the DAD2 breakout board not being used, but there is likely resistance internal to the DAD2 that was unaccounted for. The lower cutoff frequency was measured to be 424Hz, versus a simulated value of 525Hz. This is a 21.3% difference and can be explained by capacitor tolerance values and parasitic capacitance from the breadboard and the transistor. The capacitors used were 10% tolerance, leaving ample room for variations large enough to cause noticeable changes. Additionally, the transistor has its own capacitance that likely affected expected cutoff frequency values. The gain with a 100kΩ load was much closer to it's expected value. The gain was measured to be 36.3dB versus a simulated value of 37.690dB. This is only a 3.8% difference. As expected, a larger load resistance in comparison to the output resistance of the amplifier results in a more accurate overall circuit gain. The lower cutoff frequency was also closer to expected values. The lower cutoff frequency was measured to be 298.1Hz, versus a simulated value of 308Hz. This is only a 3.3% difference. This value is well below the specified limit of 1kHz. The common gate amplifier properly amplifies AC signals applied at it's input and meets it's lower cutoff frequency specification. Table VII shows summarizes the measurements at each stage of the experiment. R_{SIG} is assumed to be 0Ω for all measurements taken.

Measurement	Design	Simulations	Measurements
Unloaded Voltage Gain (dB)	43	38.318	NA
1kΩ Loaded Voltage Gain (dB)	—	20.515	17.34
100kΩ Loaded Voltage Gain (dB)	—	37.690	36.3
1kΩ Loaded Low Cutoff Frequency (Hz)	<1000	525	424
100kΩ Loaded Low Cutoff Frequency (Hz)	<1000	308	298.1

TABLE VII
Comparison of the common gate amplifier voltage gain and low cutoff frequency for each stage of the experiment.

5.1 Sources of Error

Much of the error observed in each circuit can be attributed to component tolerance values. Components are never exactly as advertised, and especially with 10% capacitors, values can noticeably change with these variations. Additionally, the cutoff frequency errors in the common gate amplifier can be explained by the gate capacitance of the 2N7000 MOSFET. There is also likely human error involved, as both circuits were based on circuit built in Experiment 4. This likely introduced error with matching parts to the previous circuits.

6 Conclusions

Throughout this experiment the design, simulation, construction and measurement of a common emitter amplifier as well as a common gate amplifier are executed. By following the steps provided in the lab manual.[1], constructing both a common gate and common emitter amplifier was made possible. Prior to the beginning of this experiment neither members of the team had gone through the steps needed to complete a common emitter amplifier nor a common gate amplifier. As this was a learning experience and the measured results were within the margin of error of the expected value, it is reasonable to say the goals of this experiment were achieved.

References

[1] N. Emanetoglu, “Laboratory experiment #4: Single transistor amplifiers,” University of Maine, Orono, ME, USA, 2020.